TrueTime

Model 560-5183-3
QUAD Digital to FM Fiber Optic Transmitter
Manual

January 8, 1999

Serial Number _____

SECTION ONE

1 FUNCTIONAL DESCRIPTION

1.1 PURPOSE OF EQUIPMENT

The TrueTime 560-5183-3 card is configured to provide four fiber optic outputs. The card, with four fiber optic connectors, occupies a rear slot.

The signal source for the card is one of the timing signals that is distributed via INPUT 1 through INPUT 8 on the Model 56000 backplane. The card is configured at installation by DIP switches to select the signal that will be the Primary and Secondary input.

The Primary and Secondary inputs are monitored for activity. The activity on both inputs is compared to the Delay switch time-out setting (user settable DIP switch SW3) which operates as a watch dog timer. If activity on either the Primary or the Secondary inputs exceeds the delay switch time-out setting, that input is considered bad. NOTE: An input may be considered bad if the minimum input voltage level is not met.

The 560-5183-1 card will automatically switch to the Secondary input source when the following conditions are met:

1. The Secondary input is good (activity time-out not exceeded).
2. The Primary input is bad (activity time-out exceeded).

The card will not switch to the Secondary input source if it has been detected bad. The card will switch back to the Primary input signal source only after the Primary input has been qualified good (good for 1 minute). This feature restores the card to normal operation automatically.

1.2 PRIMARY/ SECONDARY SIGNAL SELECT FUNCTIONS

If the 560-5183-3 is operating using the Primary input signal and it detects inactivity on this input, the 560-5183-3 card will automatically switch to the Secondary input signal.

1.3 PHYSICAL SPECIFICATIONS

Dimensions:	0.8”w X 3.94”h X 8.66”d (2 cm X 10 cm X 22 cm)
Weight:	Approximately ½ pound (¼ kg)

1.4 ENVIRONMENTAL SPECIFICATIONS

Operating Temp:	0° to +50°C
Storage Temp:	-40° to +85°C
Humidity:	Up to 95% relative, non-condensing
Cooling Mode:	Convection

1.5 POWER REQUIREMENTS

Voltage:	18-72 VDC
Power:	3.5 W

1.6 FUNCTIONAL SPECIFICATIONS

1.6.1 INPUT 1 THROUGH 8

Logic Input Level:	Low: -5 V < Vin < 1.2 V / High: 1.8 V < Vin < 5.0 V
Impedance:	>20k Ohms
Frequency:	DC to 100 kpps

1.6.2 FIBER OPTIC OUTPUTS

Quantity:	4
Connector Type	ST
Signal:	820 nm, -14 to -21 dBm into 50/125 micron fiber
Signal:	820 nm, -10 to -18 dBm into 62.5/125 micron fiber
Bandwidth	1 Hz to 100 KHz
Signal Delay:	<1 us

1.6.3 CARD COMPATIBILITY

Location:	Slot 1-17, rear
Compatibility:	See Card Compatibility Matrix

SECTION TWO

2 INSTALLATION AND OPERATION

2.1 HOT SWAPPING

All cards, input cables and output cables are hot swappable. It is not necessary to remove chassis power during insertion or removal. Hot swapping and reference-source changes are abrupt, the effects difficult to characterize; however, the system is designed to protect against permanent effects and minimize temporary effects of these events.

Typically, adjacent-card hot swapping has a negligible effect on the Digital output card. The effect of redundant power supply switch-over is also negligible.

2.2 REMOVAL AND INSTALLATION

CAUTION: Individual components on this card are sensitive to static discharge. Use proper static discharge procedures during removal and installation.

Refer to CARD COMPATIBILITY section prior to installing new card. To remove card, loosen the captive retaining hardware at the top and bottom of the assembly, then firmly pull on the handle (or on any connector on rear panel adapter cards) at the bottom of the card. Slide the card free of the frame. Refer to the SETUP section for any required switch settings; or, set them identically to the card being replaced. Reinstall the card in the frame by fitting it into the card guides at the top and bottom of the frame and sliding it in slowly, avoiding contact between bottom side of card and adjacent card front panel, until it mates with the connector. Seat card firmly to avoid contact bounce. Secure the retaining screws at the top and bottom of the card assembly.

2.3 SETUP

The setup of the 560-5183-3 digital output card involves selection of the following DIP switches:

1. Primary input select switch (SW5)
2. Secondary input select switch (SW6)
3. Primary input enable switch (SW1)
4. Secondary input enable switch (SW2)
5. Delay switch (activity time-out) (SW3)

2.3.1 REQUIRED SETTINGS (SW3)

SW3-4 MUST be OFF

2.3.2 PRIMARY INPUT SOURCE SELECT SWITCH (SW5)

Set one SW5 switch to the ON position. The SW5 switch number (1 thru 8) corresponds to INPUT 1 thru INPUT 8 signals that are distributed on the Model 56000 backplane.

2.3.3 SECONDARY INPUT SOURCE SELECT SWITCH (SW6)

Set one SW6 switch to the ON position. The SW6 switch number (1 thru 8) corresponds to INPUT 1 thru INPUT 8 signals that are distributed on the Model 56000 backplane.

2.3.4 PRIMARY INPUT ENABLE SWITCH (SW1)

This switch is readable by the Fault Monitor CPU card which can provide status information to the user. This switch MUST be set to a binary representation of the SW5 setting, the Primary input signal switch.

Primary Input	SW1-1	SW1-2	SW1-3	SW1-4
INHIBIT	OFF	OFF	OFF	OFF
INPUT 1	ON	OFF	OFF	OFF
INPUT 2	OFF	ON	OFF	OFF
INPUT 3	ON	ON	OFF	OFF
INPUT 4	OFF	OFF	ON	OFF
INPUT 5	ON	OFF	ON	OFF
INPUT 6	OFF	ON	ON	OFF
INPUT 7	ON	ON	ON	OFF
INPUT 8	OFF	OFF	OFF	ON

This switch is also used to disable the Primary input. If SW1 switches 1 thru 4 are OFF, the card will inhibit operation and fault reporting of the Primary input.

2.3.5 SECONDARY INPUT ENABLE SWITCH (SW2)

This switch is readable by the Fault Monitor CPU card which can provide status information to the user. This switch MUST be set to a binary representation of the SW6 setting, the Secondary input signal switch.

Secondary	SW2-1	SW2-2	SW2-3	SW2-4
INHIBIT	OFF	OFF	OFF	OFF
INPUT 1	ON	OFF	OFF	OFF
INPUT 2	OFF	ON	OFF	OFF
INPUT 3	ON	ON	OFF	OFF
INPUT 4	OFF	OFF	ON	OFF
INPUT 5	ON	OFF	ON	OFF
INPUT 6	OFF	ON	ON	OFF
INPUT 7	ON	ON	ON	OFF
INPUT 8	OFF	OFF	OFF	ON

This switch is also used to disable the Secondary input. If SW2 switches 1 thru 4 are OFF, the card will inhibit operation and fault reporting of the Secondary input.

2.3.6 DELAY SWITCH (Activity Time-Out SW3 Switches 1 Thru 3)

SW3 switches 1 thru 3 are used to set the input activity time-out delay. The user should set the delay for a time-out value that is the closest to but longer than the period of the input signal. This will provide fault detection in the shortest amount of time (Primary to Secondary switch-over time is minimized).

Example Setting: If the input signal is 1 kpps (1 millisecond period), the appropriate setting would be SW3-1 ON, SW3-2 OFF, SW3-3 OFF --(2.048 millisecond time-out).

Delay (time-out)	SW3-1	SW3-2	SW3-3
204.8 microseconds	OFF	OFF	OFF
2.048 milliseconds	ON	OFF	OFF
20.48 milliseconds	OFF	ON	OFF
204.8 milliseconds	ON	ON	OFF
2.048 seconds	OFF	OFF	ON
20.48 seconds	ON	OFF	ON
122.88 seconds	OFF	ON	ON
INFINITE	ON	ON	ON

If infinite delay has been selected, Primary and Secondary input fault detection is disabled.

2.4 FAULT STATUS INDICATIONS

This card has no external LED fault indicators.

2.4.1 INIT. FAULT INDICATOR

This is an on-card fault indicator which is not externally visible; although it can be seen by installing the card next to an empty slot. It indicates a failure of the card to initialize properly during power-up. Occasionally, this fault is caused by a temporary condition related to the cycling of power and can be cleared by a power or hot swap cycle. If this is unsuccessful, the card is defective.

SECTION THREE

3 THEORY OF OPERATION

3.1 GENERAL INFORMATION

This section contains a description of the circuits in the 560-5183-3 Fiber Optic Output card.

3.2 HARDWARE DESCRIPTION

The 560-5183-3 Digital Output card incorporates Primary and Secondary signal input source switches, a DC-to-DC Converter, four output drivers driving 4 LEDs into fiber optic connectors, and input fault-detection circuitry.

3.3 DETAILED DESCRIPTION

Reference drawing 560-5183.

3.3.1 PRIMARY AND SECONDARY INPUTS

The Primary Input select switch and the Secondary Input select switch each direct the signal on backplane, INPUT 1 thru INPUT 8, to an analog buffer, then to an analog multiplexer. One of the eight switches should be in the ON position. The analog signals from the Primary and Secondary inputs are compared to a voltage level of 0.9 volts via comparators which are used to detect activity. The input level on the Primary and Secondary inputs should be a minimum of 2 Vpp or the Primary and Secondary input activity detection circuitry may indicate a loss of signal. Under normal operation, the analog multiplexer output is either the buffered Primary input signal or the buffered Secondary input signal depending on the state of the analog switch control.

3.3.2 POWER SUPPLY

The DC-to-DC Converter converts 48 VDC backplane power to local ±5 VDC power. It is fully-isolated from the backplane power and referenced to signal GND on the Analog output card. Backplane power is supplied via a Polyswitch fuse device, diode and Pi-section L-C filter. The poly-fuse protects the backplane power bus from internal DC-to-DC shorts. The diode and L-C filter serve a triple purpose. During live-insertion, the high-current inductor minimizes in-rush current to the DC-to-DC being inserted; and, the diode and capacitor serve to hold up the local voltage at the input to each currently-installed DC-to-DC. During steady-state conditions, the L-C filter minimizes switching noise coupled back into the backplane power bus. During live-extraction, the 0.1 uF capacitor absorbs the inductive-kick of the opened circuit, minimizing contact-arcing. The -5 VDC side of the supply is artificially loaded, providing a minimum load to improve output voltage regulation. The power-up reset generator, assures that

RESET is active while the +5 VDC supply is between 1 and 4.5 VDC. This guarantees proper configuration of the Xilinx FPGA during hot swapping and power-up.

3.3.3 FPGA

A Field Programmable Gate Array is the interface between the card and the CPU (if installed). The FPGA provides the timing and control signals for the card.

3.3.4 FAULT INDICATION

The INIT. FAULT indicator is driven by the FPGA Initialization-done signal. It activates during initialization, and remains active if initialization does not complete. This is an extremely unusual occurrence.

SECTION FOUR

4 DETAILED DRAWINGS

4.1	560-5183	DETAILED DRAWINGS
4.2	560-5183-3	BILL OF MATERIALS